CLAIMS

What is claimed is:

1. A semiconductor structure comprising:

a substrate material and a composite laminate dielectric layer formed on the substrate material, the composite laminate dielectric layer comprising;

a layer of ZrO_2; and

a layer of a lanthanide oxide on the ZrO_2 layer.

2. The semiconductor structure of claim 1 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

3. The semiconductor structure of claim 1 wherein the composite laminate dielectric layer is a gate dielectric layer of a transistor.

4. The semiconductor structure of claim 3 wherein the transistor is a component of a DRAM.

5. The semiconductor structure of claim 1 wherein the composite laminate dielectric layer is a dielectric layer of a capacitor.

6. The semiconductor structure of claim 5 wherein the capacitor is a component of a DRAM.

7. The semiconductor structure of claim 1 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

8. The semiconductor structure of claim 1 wherein the ZrO_2 layer has a thickness of about 1–6 nm.

9. The semiconductor structure of claim 1 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

10. The semiconductor structure of claim 1 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

11. The semiconductor device of claim 1 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

12. The semiconductor device of claim 1 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

13. A semiconductor transistor comprising:

a gate electrode;

a source region and a drain region; and

a gate dielectric layer beneath the gate electrode and between the source and the drain regions, the dielectric layer being a composite laminate dielectric layer comprising a first layer of ZrO_2 and a second layer of lanthanide oxide.

14. The semiconductor transistor of claim 13 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

15. The semiconductor structure of claim 13 wherein the ZrO_2 layer has a thickness of about 2–5 nm.

16. The semiconductor structure of claim 13 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

17. The semiconductor structure of claim 13 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

18. The semiconductor structure of claim 1 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

19. The semiconductor structure of claim 1 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

20. The semiconductor structure of claim 13 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

21. A semiconductor capacitor comprising:

a first electrode;

a second electrode, and

a dielectric layer separating the first and the second electrodes, the dielectric layer being a composite laminate dielectric layer comprising a first layer of ZrO_2 and a second layer of lanthanide oxide.

22. The semiconductor capacitor of claim 21 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

23. The semiconductor structure of claim 21 wherein the ZrO_2 layer has a thickness of about 1-6 nm

24. The semiconductor structure of claim 21 wherein the ZrO_2 layer has a thickness of about 1-2 nm.

25. The semiconductor structure of claim 21 wherein the ZrO_2 layer has a thickness of about 3 nm.

26. The semiconductor capacitor of claim 21 wherein the lanthanide oxide layer has a thickness of about 2-4 nm

27. The semiconductor capacitor of claim 21 wherein the lanthanide oxide layer has a thickness of about 3 nm

28. The semiconductor capacitor of claim 21 wherein the composite laminate dielectric layer has a thickness of about 9 nm.

29. The semiconductor capacitor of claim 21 wherein the ZrO_2 layer is formed by atomic layer deposition from a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

30. The semiconductor capacitor of claim 21 wherein the lanthanide oxide layer is formed by electron beam evaporation of a lanthanide oxide.

31. The semiconductor capacitor of claim 21 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

32 A semiconductor memory device comprising:

a capacitor that includes a first dielectric material separating a first and a second electrode;

a transistor that includes a second dielectric material beneath a gate electrode and between a source and a drain region, and

at least one of the first and second dielectric materials is a composite laminate dielectric layer comprised of a first layer of material selected from the group consisting of ZrO_2 and lanthanide oxide and a second layer of material selected from the group consisting of ZrO_2 and a lanthanide oxide on the first layer of material, the second layer of material being different from the first layer of material.

33. The semiconductor memory device of claim 32 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

34. The semiconductor memory device of claim 32 wherein the first dielectric material is comprised of the composite laminate dielectric layer.

35. The semiconductor memory device of claim 32 wherein the second dielectric material is comprised of the composite laminate dielectric layer.

36. The semiconductor memory device of claim 32 wherein the wherein each of the first and the second dielectric material is comprised of the composite laminate dielectric layer.

37. The semiconductor memory device of claim 32 wherein the device is a DRAM.

38. The semiconductor memory device of claim 32 wherein the composite laminate dielectric layer has a dielectric constant between about 12 and about 23.

39. The semiconductor memory device of claim 32 wherein the ZrO_2 layer has a thickness of about 1–6 nm.

40. The semiconductor memory device of claim 32 wherein the lanthanide oxide layer has a thickness of about 2 –12 nm.

41. The semiconductor memory device of claim 32 wherein the composite laminate dielectric layer has a thickness of about 3-18 nm.

42. A method of forming a composite laminate dielectric layer for a semiconductor structure, comprising

forming a first layer of a material selected from the group consisting of ZrO_2 and lanthanide oxide on a substrate; and

forming a second layer of material selected from the group consisting of ZrO_2 and a lanthanide oxide on the first layer of material, the second layer of material being different from the first layer of material.

43. The method of claim 42 wherein the first layer of material is ZrO_2 and the second layer of material is the lanthanide oxide.

44. The method of claim 42 wherein the first layer of material is the lanthanide oxide and the second layer of material is ZrO_2.

45. The method of claim 42 wherein the lanthanide oxide is selected from the group consisting of Pr_2O_3, Nd_2O_3, Sm_2O_3, Gd_2O_3, Dy_2O_3 and PrTixOy.

46. The method of claim 42 wherein depositing the ZrO_2 is performed at a temperature of about 230-325 °C.

47. The method of claim 42 wherein the act of depositing the ZrO_2 oxide includes atomic layer deposition of a ZrI_4 precursor followed by oxidation with H_20/H_2O_2.

48. The method of claim 47 wherein the atomic layer deposition is performed at a temperature of about 230 - 325 °C.

49. The method of claim 47 wherein the atomic layer deposition is performed at a temperature of about 272-275 °C.

50. The method of claim 42 wherein the lanthanide oxide layer is formed by electron beam evaporation of the lanthanide oxide.

51. The method of claim 42 wherein the ZrO_2 oxide layer is formed by atomic layer deposition of a ZrI_4 precursor followed by oxidation with H_20/H_2O_2 and the lanthanide oxide layer is formed by electron beam evaporation of the lanthanide oxide.

52. The method of claim 42 wherein the ZrO_2 layer is formed to a thickness of about 2-5 nm.

53. The method of claim 42 wherein the lanthanide oxide layer is formed to a thickness of about 2-10 nm.

54. The method of claim 42 wherein the ZrO_2 layer is formed to a thickness of about 2-5 nm and the lanthanide oxide layer is formed to a thickness of about 2-10 nm.